ABSTRACT

A method and a processor for processing a power mode instruction are provided. The power mode instruction itself includes up to five different sleep modes and one run mode, each for initiating a clock source change or inhibit. This instruction may be executed in one processor cycle and with one power mode instruction employing clock transition logic within the processor to initiate a switch to the clock source configuration specified by a literal, such as a 3-bit literal. Operand may be written the register of clock transition logic to define an exit state for a sleep mode.